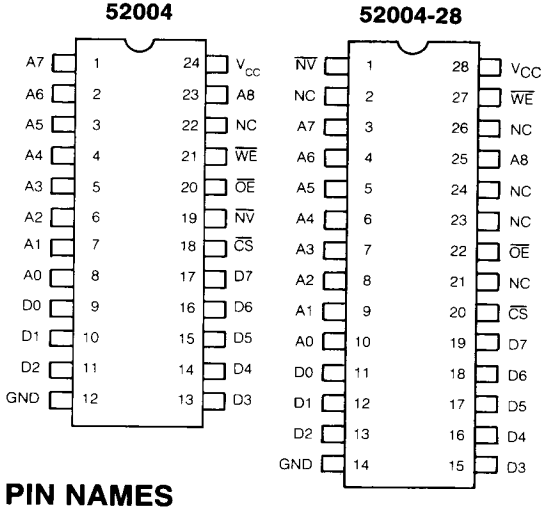
52004
4K BIT (512 x 8)NVRAM

PRELIMINARY

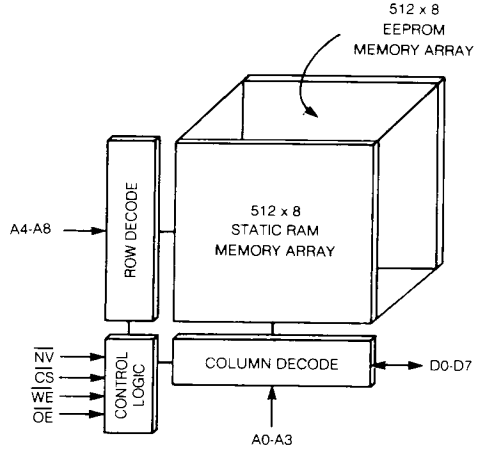
- **4K Bit Static RAM backed by 4K Bit Electrically Erasable PROM**
- **Fully 5V Only Operation**
- **Directly TTL Compatible**
- **In Circuit EEPROM Changes**
- **SRAM Cycle Time less than 300 ns**
- **Power-Failure Protection**
- **Unlimited Recall Cycles**
- **Memory Margining Capability**
- **Operating ranges**
  52004 ..... 0°C to +70°C
  52004I ..... –40°C to +85°C
  52004HR ..... –55°C to +125°C

The NCR 52004 non-volatile RAM combines 4K (512 × 8) bits of conventional static RAM (SRAM) with an identical size array of Electrically Erasable PROM (EEPROM). Non-volatile data can be stored in the EEPROM while independent data is accessed simultaneously in the SRAM. Data can be transferred back and forth between the SRAM and the EEPROM by simple Store and Recall operations. A non-volatile Store signal transfers data from the SRAM to the non-volatile EEPROM where it is safely stored even when power is removed. When power is restored, the data in the EEPROM is automatically recalled into the SRAM. Data stored in the non-volatile EEPROM can be recalled an unlimited number of times. The NCR 52004 requires only a single 5 volt power supply for all modes of operation, and is completely TTL compatible with fully static timing and three state outputs. The NCR 52004 is available in a 24 pin package and an optional 28 pin package, in commercial, industrial and high reliability versions.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A0-A8	Address Inputs	$\overline{WE}$	Write Enable
D0-D7	Data I/0	$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select	NC	No Connection
$\overline{NV}$	Non-Volatile Enable	V_{CC}	+5 Volts ±10%

This is advance information and NCR reserves the right to change the specifications without notice.

DEVICE OPERATION

SRAM READ/WRITE

The NCR 52004 can be read like a conventional static RAM. With $\overline{CS}$ and $\overline{OE}$ low and $\overline{WE}$ high, valid data will be presented to output pins. With $\overline{CS}$ and $\overline{WE}$ low, and $\overline{OE}$ high, the SRAM can be written to like a conventional static RAM.

STORE

Transferring data from the SRAM to the non-volatile EEPROM is controlled by the Store operation. The $\overline{NV}$ input signal controls the non-volatile operations (i.e., Store and Recall), except for automatic data recall upon power up. When $\overline{NV}$ and $\overline{WE}$ are brought low, the entire contents of the SRAM array are copied into the non-volatile EEPROM array. The data in the SRAM is unaffected by a Store operation. The Recall cycle is inhibited by a Store operation, and $\overline{CS}$ can either be high or low.

The I/0 terminals are in the high impedance state during a Store operation. The contents of the EEPROM remain valid with or without power being supplied. The data retention time of the EEPROM can be measured by memory margining.

During power up or power down, precaution must be taken to prevent an unintentional Store cycle. Holding $\overline{NV}$ high will inhibit the initiation of a Store cycle. Additionally, a Store operation should not be initiated until the supply voltage (V_{CC}) is at specification limits.

RECALL

The data stored in the non-volatile EEPROM array is transferred back into the SRAM by the Recall operation. When $\overline{NV}$ and $\overline{OE}$ are brought low, the entire contents of the EEPROM are copied back into the SRAM (overwriting any data already existing in the SRAM). An Array Recall cycle can take place when $\overline{CS}$ is either high or low. An array Recall operation will automatically be performed upon power up. The data in the EEPROM is unaffected by a Recall operation.

The Data I/0 terminals are in a high impedance state during a non-volatile operation (i.e., Store or Recall). When a non-volatile cycle is initiated, all other operations are inhibited until the first operation is complete.

MEMORY MARGINING

The NCR 52004 supports margining of the memory transistors. Memory margining allows device retention time to be projected for the purpose of device evaluation. An application note describing the memory margining algorithm is available.

MODE SELECTION

	INPUTS			
MODE	$\overline{CS}$	$\overline{NV}$	$\overline{WE}$	$\overline{OE}$
READ	L	H	H	L
WRITE	L	H	L	H
STORE	X	L	L	H
RECALL	X	L	H	L

ABSOLUTE MAXIMUM RATINGS

All inputs or outputs relative to Vss . . . . . – 0.5 to + 7V
Storage temperature without
data retention . . . . . –65°C to + 150°C

Stress above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operational limits stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	52004			52004I			52004HR**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	Input high level voltage	2.0		V_{CC}	2.0		V_{CC}	2.0		V_{CC}	V
V_{IL}	Input low level voltage	–0.3		0.8	–0.3		0.8	–0.3		0.8	V
T_A	Ambient Temperature	0		70	–40		85	–55		125	°C

All voltages are with respect to GND.

STATIC ELECTRICAL CHARACTERISTICS, OVER RECOMMENDED OPERATION CONDITIONS (UNLESS OTHERWISE NOTED)

Symbol	Parameter	Condition	52004			52004I			52004HR**			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{IN}	Input leakage current	V_{IN} = 0V TO 5.5V		0.1	10		0.1	10		0.1	10	μA
I_O	I_O leakage current	V_O = 0.4V TO 5.5V Chip Deselected		0.1	10		0.1	10		0.1	10	μA
I_{CC}	Supply Current	Outputs Open		35	70		45	80		45	80	mA
V_{OH}	Output High Voltage	I_{OH} = –400μA	2.4			2.4			2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA			0.4			0.4			0.4	V
T_S	Non-Volatile storage time		TBD									yr

*Typical values are at 25°C and typical supply voltages.

CAPACITANCE $T_A = 25°C$, f = 1.0 MHz, $V_{CC} = 5V$

Symbol	Parameter	Condition	52004			52004I			52004HR**			Unit
			Min	Typ	Max	Min	Typ*	Max	Min	Typ	Max	
C	Capacitance of Input & Data I/O pins	All pins at VSS (ground)			10			10			10	pF

* *The 52004HR Data is preliminary and is subject to change.

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AC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

READ CYCLE

Symbol	Parameter	52004			52004I			52004HR**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{RC}	Read Cycle Time	300			300			450			ns
t_{ACC}	Address Access Time			300			300			450	ns
t_{A}	Chip Select or Output Enable to Data Active	0			0			0			ns
t_{OE}	Output Enable Time			100			120			120	ns
t_{CS}	Chip Select Access Time			100			120			120	ns
t_{OH}	Output Hold Time	10			10			10			ns
t_{OZ}	Chip Select Or Output Enable To Output High Impedance Time			90			90			90	ns

WRITE CYCLE

Symbol	Parameter	52004			52004I			52004HR**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{WC}	Write Cycle Time	300			300			450			ns
t_{W}	Write Pulse Width	150			150			300			ns
t_{WR}	Write Release Time	25			25			25			ns
t_{DW}	Data to Write Time Overlap	150			150			200			ns
t_{DH}	Data Hold From Write Time	20			20			20			ns
t_{AS}	Address Setup Time	50			50			50			ns

STORE CYCLE

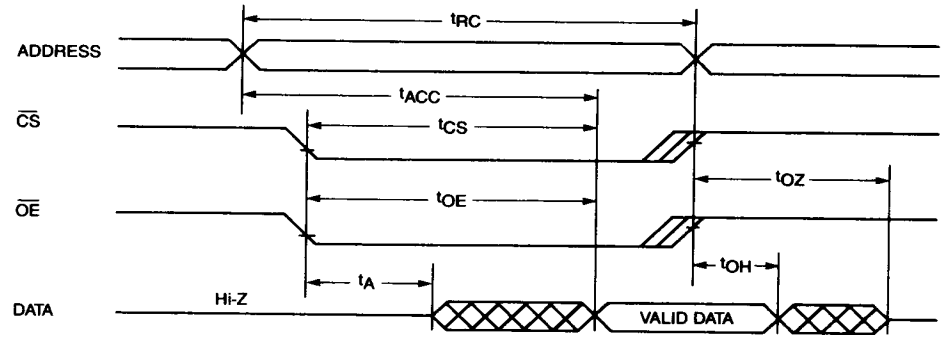
Symbol	Parameter	52004			52004I			52004HR**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{STC}	Store Cycle Time			10			10			10	ms
t_{NW}	NV to Write Overlap	100			100			100			ns
t_{NS}	NV Setup Time	0			0			0			ns
t_{STZ}	Store to Output Hi-Z			100			100			100	ns
t_{SC}	Number of Store Cycles	10^4			10^4			10^4			cycle

RECALL CYCLE

Symbol	Parameter	52004			52004I			52004HR**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{RCC}	Array Recall Cycle Time			20							μs
t_{NO}	NV to Output Overlap	200			450			450			ns
t_{NS}	NV Setup time	0			0			0			ns
t_{RCZ}	Recall to Output Hi-Z			100			100			100	ns

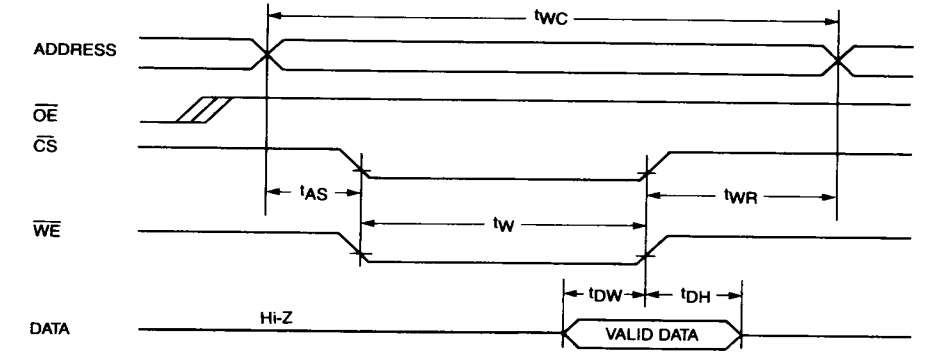
**The 52004HR Data is preliminary and is subject to change.

READ CYCLE



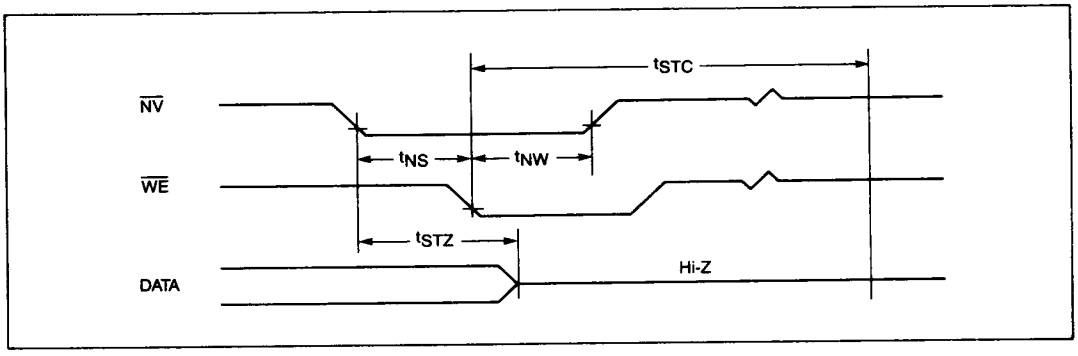
NOTE: During a read operation $\overline{WE}$ should be held at V_{IH}.

WRITE CYCLE

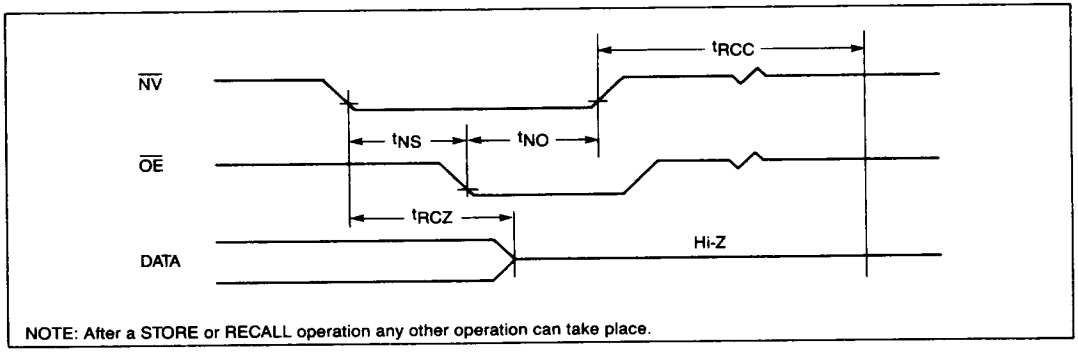


NOTE: $\overline{WE}$ may be asserted prior to $\overline{CS}$. t_{AS} applies to $\overline{CS}$ or $\overline{WE}$ whichever occurs last.

STORE CYCLE



RECALL CYCLE

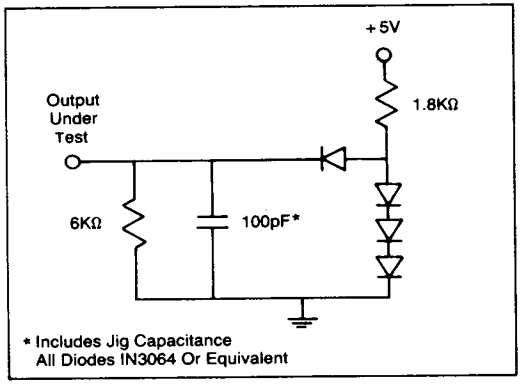


NOTE: After a STORE or RECALL operation any other operation can take place.

A. C. CONDITIONS OF TESTS

Input Pulse Levels . . . . . 0.8 Volts to 2.0 Volts
Input Rise & Fall Times . . . . . 10 nsec
Output Timing Levels . . . . . 0.8 Volts to 2.0 Volts

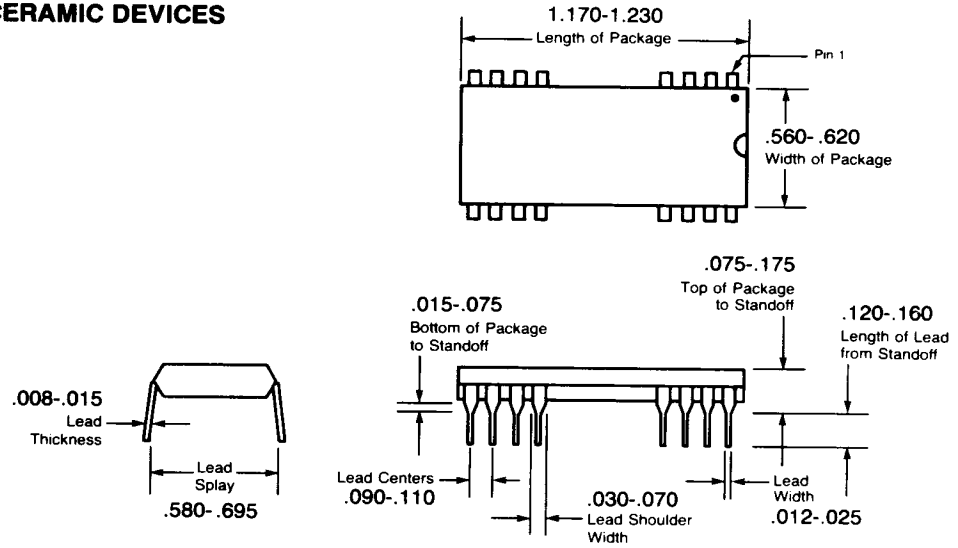
TEST LOAD CIRCUIT



* Includes Jig Capacitance
All Diodes IN3064 Or Equivalent

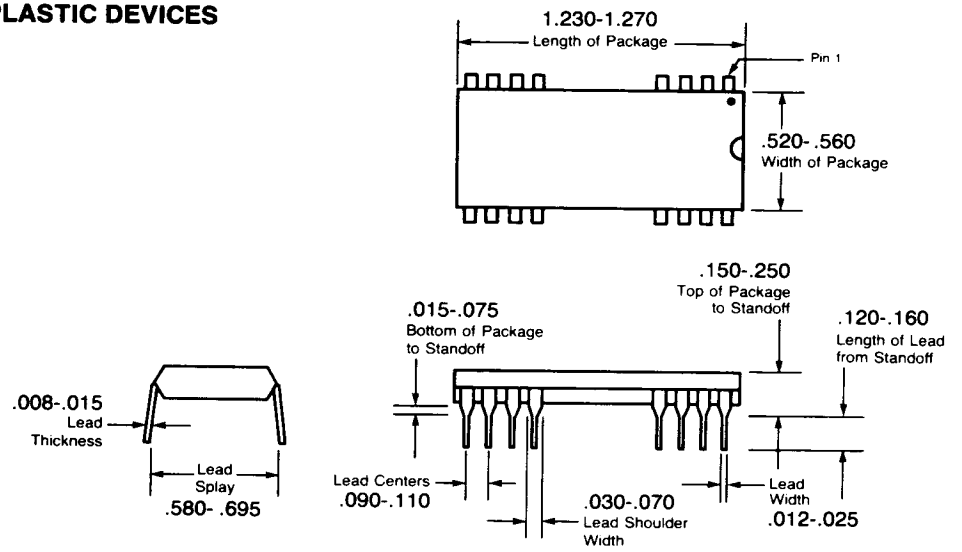
MECHANICAL DATA 24 PIN

CERAMIC DEVICES



All dimensions are inches.

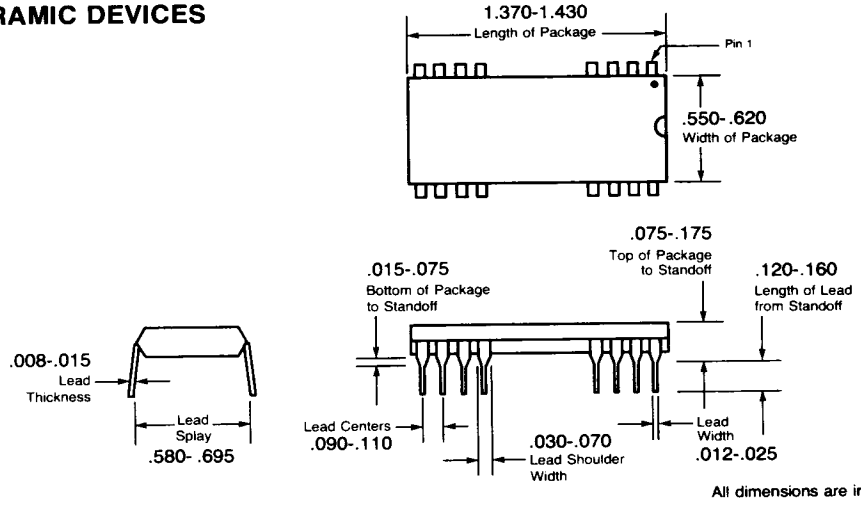
PLASTIC DEVICES



All dimensions are inches.

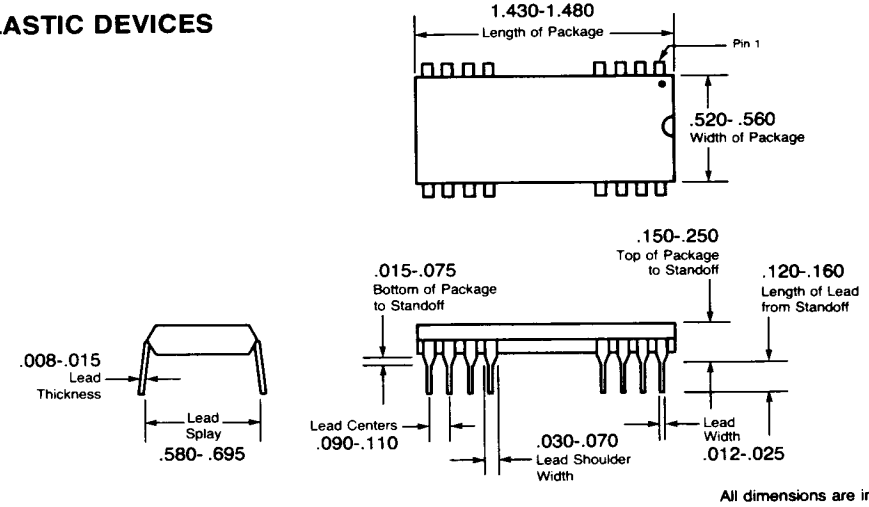
MECHANICAL DATA 28 Pin

CERAMIC DEVICES



All dimensions are inches.

PLASTIC DEVICES



All dimensions are inches.

NCR

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