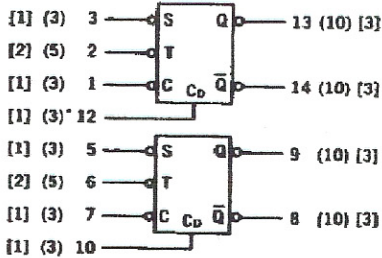


DUAL J-K FLIP-FLOPS

PLASTIC MRTL MC700P/800P series

MC790P • MC890P

Two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.



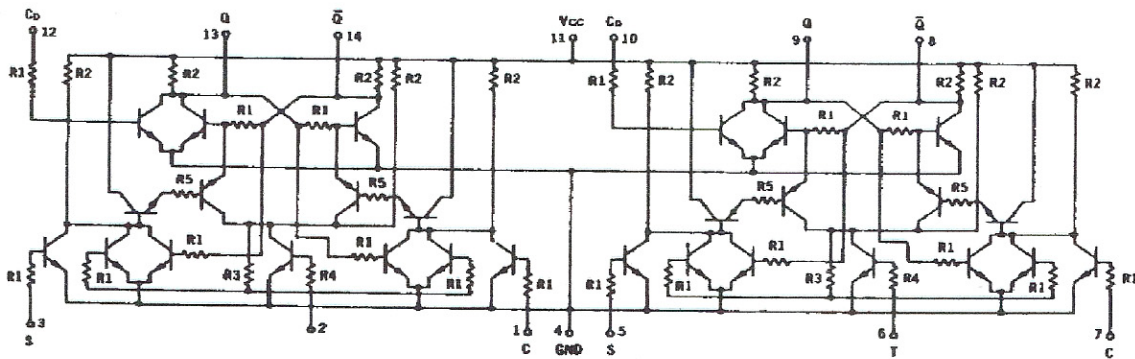
$f_{max} = 4 \text{ MHz}$
 $P_D = 182 \text{ mW}$ (Only Clock Input High)
 158 (Inputs Low)

NUMBER IN PARENTHESES INDICATES LOADING FACTOR FOR mW MRTL
 NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MRTL

CLOCKED INPUT OPERATION

t_n (2)	$t_n + t$ (2)	Q	\bar{Q}
S	C	Q _n (3)	\bar{Q}_n (3)
1	1	1	0
1	0	1	0
0	1	0	1
0	0	\bar{Q}_n (3)	Q _n (3)

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n , and the time period subsequent to this transition is denoted t_{n+t} .
3. Q_n is the state of the Q output in the time period t_n .
4. Clock pulse fall time must be $< 100 \text{ ns}$.



TYPICAL RESISTANCE VALUES
 $R1 = 450 \Omega$ $R3 = 510 \Omega$
 $R2 = 640 \Omega$ $R4 = 225 \Omega$
 $R5 = 300 \Omega$

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only.
The other flip-flop is tested in the same manner.

		TEST VOLTAGE VALUES				
		(Volts)				
⊗ Test Temperature		V _{in}	V _{on}	V _{DET}	V _{off}	V _{CE}
MC890P	0°C	0.860	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC790P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

Characteristic	Symbol	Pin Under Test	MC890P Test Limits						MC790P Test Limits						TEST VOLTAGE APPLIED TO PINS LISTED BELOW:					Gnd		
			0°C		+25°C		+75°C		+15°C		+25°C		+55°C		V _{in}	V _{on}	V _{DET}	V _{off}	V _{CE}			
			Min	Max	Min	Max	Min	Max	Unit	Min	Max	Min	Max	Min							Max	Unit
Input Current	I _{in}	1	-	600	-	600	-	570	μA _{dc}	-	500	-	500	-	470	μA _{dc}	1	-	13	-	11	2, 3, 4, 12
	2I _{in}	2	-	1200	-	1200	-	1140	↓	-	1000	-	1000	-	940	↓	2	-	1, 3	-	↓	4, 12
	I _{in}	3	-	600	-	600	-	570	↓	-	500	-	500	-	470	↓	3	-	14	-	-	1, 2, 4, 12
	I _{in}	12	-	600	-	600	-	570	↓	-	500	-	500	-	470	↓	12	-	14	-	-	1, 2, 3, 4
Output Current	I _{A3}	13	1.80	-	1.80	-	1.71	-	mA _{dc}	1.65	-	1.65	-	1.56	-	mA _{dc}	-	13	1	12	11	2, 3, 4
		14	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	14	3, 12	-	↓	1, 2, 4
		14	↓	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	-	12, 14	3	-	↓	1, 2, 4
Output Voltage	V _{out}	13	-	500	-	400	-	400	mV _{dc}	-	400	-	300	-	320	mV _{dc}	-	12	-	-	11	1, 2, 3, 4, 14
		13*#	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1, 3	-	-	↓	4, 12
		13*##	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1	-	3	-	↓
		13*###	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	1, 3	-	↓
		14*##	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	1, 3	-	-	1	↓
		14*#	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	3	-	-	1, 3	↓
Saturation Voltage	V _{CE(sat)}	13	-	400	-	300	-	350	mV _{dc}	-	300	-	290	-	320	mV _{dc}	-	-	12	-	11	1, 2, 3, 4, 14
		13#	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	↓	1, 2, 3, 4, 12
		14*#	-	↓	-	↓	-	↓	↓	-	↓	-	↓	-	↓	↓	-	-	12	-	↓	1, 2, 3, 4

Ground unused input pins. Other pins not listed are left open.

Pin 13 = LOW } Set by a momentary ground prior to the
Pin 14 = LOW } application of the negative-going Clock Pulse.

* Clock pulse to pin 2, see Figure 1.

FIGURE 1 — CLOCK PULSE DEFINITION

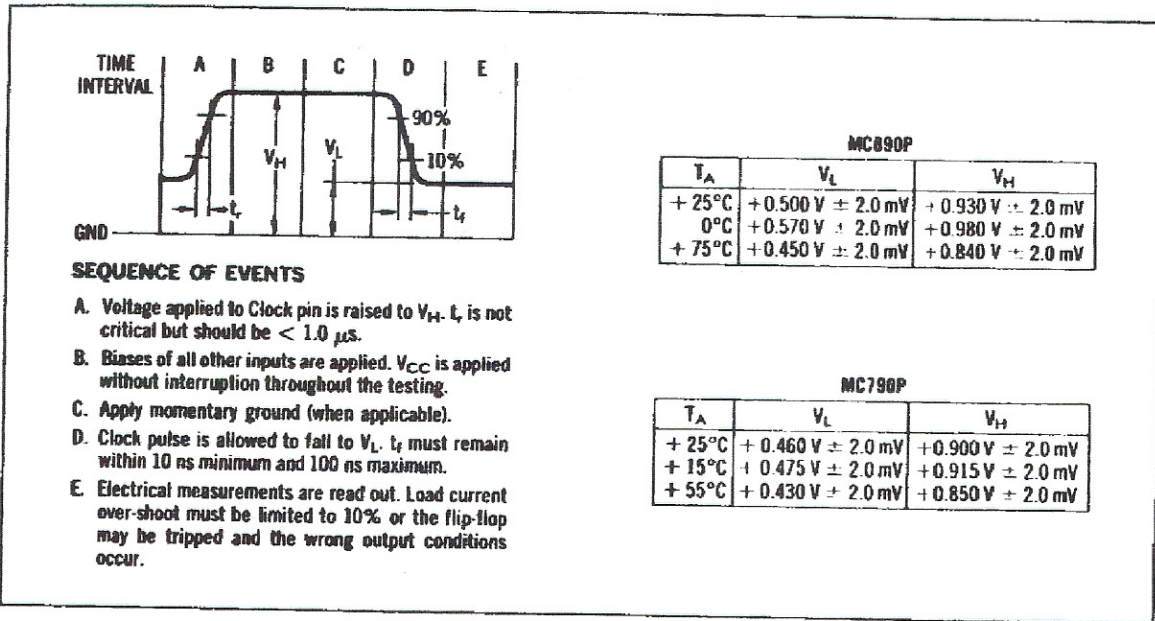


FIGURE 2 — TOGGLE MODE TEST CIRCUIT

