intel®

8708

8192/4096 BIT ERASABLE AND ELECTRICALLY REPROGRAMMABLE READ ONLY MEMORY

- ● **8708 1024x8 Organization**

- ■ **Fast Programming —
  Typ. 100 sec. For All 8K Bits**
- ■ **Low Power During Programming**
- ■ **Access Time—450 ns**
- ■ **Standard Power Supplies—
  +12V, ±5V**

- ■ **Static—No Clocks Required**
- ■ **Inputs and Outputs TTL
  Compatible During Both Read
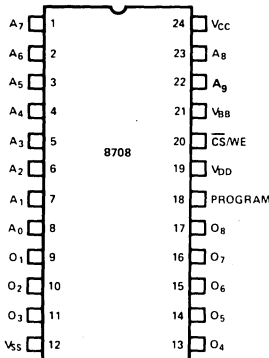 and Program Modes**
- ■ **Three-State Output—OR-Tie
  Capability**

The Intel© 8708 is a high speed 8192 bit erasable and electrically reprogrammable ROM's (EPROM) ideally suited where fast turn around and pattern experimentation are important requirements.

The 8708 is packaged in a 24 pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the devices.

A pin for pin mask programmed ROM, the Intel© 8308, is available for large volume production runs of systems initially using the 8708.

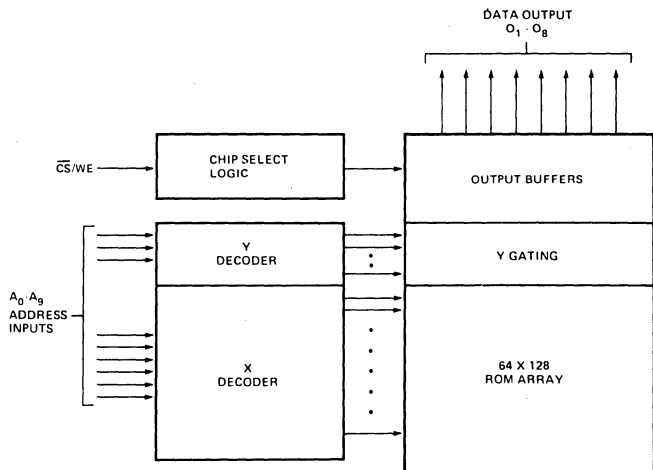The 8708 is fabricated with the time proven N-channel silicon gate technology.

PIN CONFIGURATIONS

	8708	
A_7	1	24 V_{CC}
A_6	2	23 A_8
A_5	3	22 A_9
A_4	4	21 V_{BB}
A_3	5	20 $\overline{CS}/WE$
A_2	6	19 V_{DD}
A_1	7	18 PROGRAM
A_0	8	17 O_8
O_1	9	16 O_7
O_2	10	15 O_6
O_3	11	14 O_5
V_{SS}	12	13 O_4

BLOCK DIAGRAM

PIN NAMES

A_0-A_9	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS
$\overline{CS}$/WE	CHIP SELECT/WRITE ENABLE INPUT

MCS-80

Absolute Maximum Ratings *

Temperature Under Bias . . . . -25°C to +85°C

Storage Temperature . . . . -65°C to +125°C

All Input or Output Voltages with Respect to V_{BB}

    (except Program) . . . . +15V to –0.3V

Program Input to V_{BB} . . . . +35V to –0.3V

Supply Voltages V_{CC} and V_{SS} with Respect to V_{BB} . . . . +15V to –0.3V

V_{DD} with Respect to V_{BB} . . . . +20V to –0.3V

Power Dissipation 1.5W

READ OPERATION
D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = +12V ±5%, V_{BB} = –5V ±5%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Load Current			10	μA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 5.25V, $\overline{CS}$/WE = 5V
I_{DD}	V_{DD} Supply Current		50	65	mA	Worst Case Supply Currents:
I_{CC}	V_{CC} Supply Current		6	10	mA	All Inputs High
I_{BB}	V_{BB} Supply Current		30	45	mA	$\overline{CS}$/WE = 5V; T_A = 0°C
V_{IL}	Input Low Voltage	V_{SS}		0.65	V	
V_{IH}	Input High Voltage	3.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6mA
V_{OH1}	Output High Voltage	3.7			V	I_{OH} = –100μA
V_{OH2}	Output High Voltage	2.4			V	I_{OH} = –1mA
P_D	Power Dissipation			800	mW	T_A = 70°C

NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltages.

        2. The program input (Pin 18) may be tied to V_{SS} or V_{CC} during the read mode.

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A.C. Characteristics

$T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, $V_{DD} = +12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{ACC}	Address to Output Delay		280	450	ns
t_{CO}	Chip Select to Output Delay			120	ns
t_{DF}	Chip De-Select to Output Float	0		120	ns
t_{OH}	Address to Output Hold	0			ns

Capacitance[1] $T_A = 25°C$, $f = 1MHz$

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

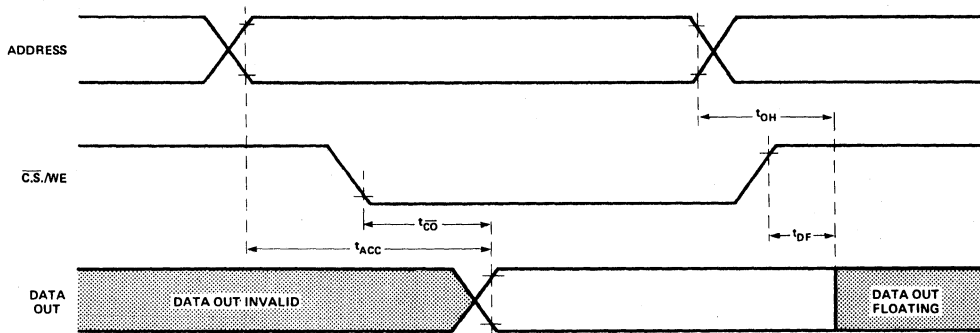Note 1. This parameter is periodically sampled and not 100% tested.

A.C. Test Conditions:

Output Load: 1 TTL gate and $C_L = 100pF$
Input Rise and Fall Times: $\leqslant 20ns$
Timing Measurement Reference Levels: 0.8V and 2.8V for inputs; 0.8V and 2.4V for outputs
Input Pulse Levels: 0.65V to 3.0V

Waveforms